FAST DECISION THRESHOLD CONTROLLER FOR BURST-MODE RECEIVER

ABSTRACT

A repetitive burst-mode input signal that has a dark time portion, a preamble portion, and a payload portion is converted into a limited output signal in accordance with a decision threshold level, which is controlled by selectively coupling an averaged value of the burst-mode data amplitude to the decision threshold level. The timing sequence for selectively coupling the averaged signal value is controlled such that the average value of the burst-mode signal acquired during the preamble portion of the burst-mode signal is applied to the decision threshold level during substantially all of the payload portion. The control circuit may incorporate a phase-locked loop, which locks onto the repetitive dark time frequency and in response synthesizes a switchable track enable signal that controls the timing sequence of the decision threshold level. The phase-locked loop can employ all-digital, analog, and/or hybrid digital/analog circuitry.

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